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Dynamic range study of common-source/Drain active balun for RF applications

FR Gomez[1], MT De Leon[2], JR Hizon[3]
[1, 2] New Product Development & Introduction Department, STMicroelectronics, Inc., Calamba City, Laguna, Philippines
[3] Microelectronics and Microprocessors Laboratory, University of the Philippines, Diliman, Quezon City, Philippines

Abstract
The paper presents a study of common-source/drain active balun circuit in terms of the dynamic range, implemented in a complementary metal-oxide semiconductor (CMOS) technology. Dynamic range can be derived using noise analysis, and is an important design consideration since it determines the susceptibility of the active balun to unwanted signal or noise. Henceforth, it is critically important that the common-source/drain active balun circuit contributes as little noise as possible in the system level design of radio frequency (RF) applications. Furthermore, design tradeoffs are inevitable and are carefully considered in the analysis and design.

Keywords: Common-source/drain active balun; dynamic range; noise analysis; CMOS; RF

1. Introduction

Active Balun Overview

A balun (balanced-unbalanced) circuit is a type of transformer that converts signals that are single-ended or unbalanced with respect to ground into signals that are differential or balanced with respect to ground, and vice versa, illustrated in Fig. 1. An ideal balun generates a pair of differential output signals of balanced amplitudes (0 dB gain difference) and phases (with 180° phase difference) from a single-ended input signal source.

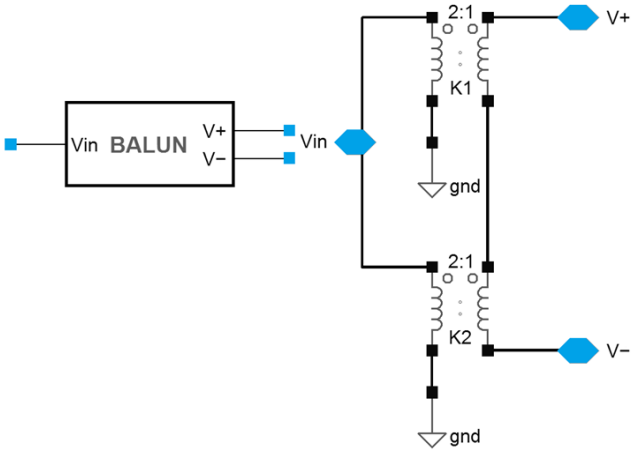

Fig 1: Typical balun transformer circuit

Baluns can be classified as either active or passive baluns depending on the devices used. Active baluns, although unidirectional and more complex to implement, are preferred over their passive counterparts because they can produce gain, occupy less chip area, and can operate at higher frequencies [1, 2]. One of the active balun topologies is the common-source/drain active balun circuit in Fig. 2, composed of a single transistor (M1) designed in complementary metal-oxide semiconductor (CMOS) technology. This active balun circuit is considered as the simplest topology amongst other active balun configurations. The input signal is fed into the gate of the transistor, and normal operation results in an inverted output signal at RFout2 and a non-inverted signal at RFout1. Ideally, the two outputs would have the same amplitude with a phase difference of 180º. Load resistors R1 and R2 determine the output voltages as well as the voltage gains of the two output signals with respect to the input signal.

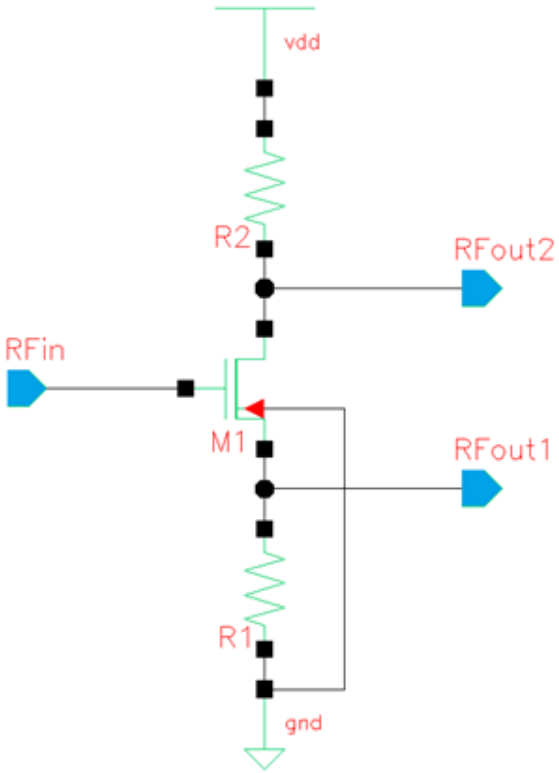

Fig 2: Common-source/drain active balun circuit schematic

Common-source topology exhibits a relatively high input impedance while providing voltage gain and requiring a minimal voltage headroom. Common-drain topology or

source-follower, on the other hand, is occasionally employed as level shifters or buffers, impacting the overall frequency response. It also exhibits high input impedance. With the two topologies merged to function as an active balun, common-drain will dominate the response on the overall voltage gain or attenuation because of the feedback effect of load resistor R1 with respect to the input.

Noise Analysis

Noise performance is an important design consideration since it determines the susceptibility of the active balun to unwanted signal or noise. Important design parameters such as the dynamic range (DR) can be derived using noise analysis. Fig. 3 shows the circuit model with noise sources of common-source/drain active balun.

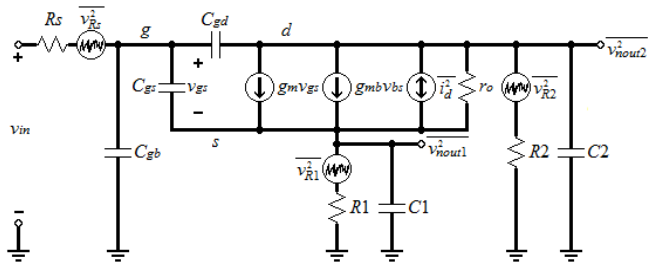

Fig 3: Common-source/drain active balun circuit model with noise generator

Since active balun supplies differential input signal into a differential circuit, noise calculation for each of the two output nodes is necessary. Succeeding discussions determine the output noise contributions of the active balun produced by the transistor itself and the output loads.

$$\overline{i_{n,out2}^2} = \overline{i_{d,th}^2} + \overline{i_{d,1/f}^2} + \overline{i_{R2}^2} + \frac{\overline{v_{Rs}^2} - \overline{v_{n,out2}^2}}{\left(1/sC_{gd}\right)^2} \quad (1)$$

$$\overline{v_{n,out2}^2} = \left[4k_BT\gamma(g_m + g_{mb})\Delta f + \frac{K_f I_D}{L^2 C_{ox}} \frac{1}{f_{co}}\Delta f + \frac{4k_BT}{R2}\Delta f + \frac{\overline{v_{Rs}^2} - \overline{v_{n,out2}^2}}{\left(1/sC_{gd}\right)^2}\right]\left(R2 \| \frac{1}{sC2}\right)^2 \quad (2)$$

At higher frequency, thermal noise of transistor dominates, hence flicker noise could be neglected. Assuming source resistance to be zero, that is Rs = 0, and rearranging (2), output voltage noise of RFout2 could be simplified.

$$\overline{v_{n,out2}^2} = \frac{k_BT}{C2} \cdot \frac{1 + \gamma(g_m + g_{mb})R2}{1 + \frac{1}{4}\left(\frac{C_{gd}}{C2}\right)^2} \quad V_{rms}^2 \quad (3)$$

Assuming that Cgd is significantly smaller than the output load capacitance C2, (3) would be simplified as

$$\overline{v_{n,out2}^2} = \frac{k_BT}{C2}[1 + \gamma(g_m + g_{mb})R2] \quad V_{rms}^2 \quad (4)$$

To verify the expression in (4), Kirchhoff's current law (KCL) at node d as earlier generated in (1) could be used with C_{gd} initially neglected. This is with the assumption that inherence capacitance C_{gd} is significantly smaller than the output capacitance C2.

$$\overline{i_{n,out2}^2} = \overline{i_{d,th}^2} + \overline{i_{d,1/f}^2} + \overline{i_{R2}^2} \quad (5)$$

$$\overline{v_{n,out2}^2} = \left[4k_BT\gamma(g_m + g_{mb})\Delta f + \frac{K_f I_D}{L^2 C_{ox}} \frac{1}{f_{co}}\Delta f + \frac{4k_BT}{R2}\Delta f\right]\left(R2 \| \frac{1}{sC2}\right)^2 \quad (6)$$

At higher frequency, thermal noise of transistor dominates, hence flicker noise could be neglected.

$$\overline{v_{n,out2}^2} = \frac{k_BT}{C2}[1 + \gamma(g_m + g_{mb})R2] \quad V_{rms}^2 \quad (7)$$

Expression for the voltage noise of RFout2 in (7) confirms that of the computation in (4). This comes with the assumption that C_{gd} is negligible as compared to C2. Interestingly, the expression for output noise power is also the signal-to-noise ratio (SNR) at the output side. Increasing the resistance R2 increases the output noise contribution. Furthermore, increasing the capacitance C2 would decrease the output voltage noise but it would also decrease the circuit bandwidth or the cutoff frequency of RFout2. This design tradeoff is inevitable so one should consider the effectiveness of setting or limiting the output capacitance.

Using the expression for SNR given as the output noise voltage in [4, 7], dynamic range of the circuit for the RFout2 side could be determined. Dynamic range is the ratio of the maximum signal power that the circuit can tolerate without distortion to noise level of circuit. Note that the largest signal that can be passed through the output of the circuit is limited by the supply voltage (V_{DD}). Dynamic range is expressed as

$$DR_2 = 10log\frac{P_{signal}}{P_{noise2}} = 20log\frac{V_{max,rms}}{V_{noise2,rms}} = 20log\frac{\frac{1}{2}\cdot\frac{V_{DD}}{\sqrt{2}}}{\sqrt{\frac{k_BT}{C2}[1 + \gamma(g_m + g_{mb})R2]}} \quad (8)$$

$$DR_2 = 10log\frac{{V_{DD}}^2 \cdot C2}{k_BT[1 + \gamma(g_m + g_{mb})R2]} \quad dB \quad (9)$$

For RFout1, the output noise voltage contribution was determined starting with KCL at node s. same assumption applies with inherent capacitance C_{gs} significantly smaller than the output capacitance C1.

$$\overline{i_{n,out1}^2} = \overline{i_{d,th}^2} + \overline{i_{d,1/f}^2} + \overline{i_{R1}^2} \quad (10)$$

$$\overline{v_{n,out1}^2} = \left[4k_BT\gamma(g_m + g_{mb})\Delta f + \frac{K_f I_D}{L^2 C_{ox}} \frac{1}{f_{co}}\Delta f + \frac{4k_BT}{R1}\Delta f\right]\left(R1 \| \frac{1}{sC1}\right)^2 \quad (11)$$

With same previous assumptions applied, expression for output voltage noise of RFout1 could be derived.

$$\overline{v_{n,out1}^2} = 4k_BT\left[\gamma(g_m + g_{mb}) + \frac{1}{R1}\right]\left(R1 \| \frac{1}{sC1}\right)^2 \Delta f \quad (12)$$

$$\overline{v_{n,out1}^2} = \frac{k_BT}{C1}[1 + \gamma(g_m + g_{mb})R1] \quad V_{rms}^2 \quad (13)$$

Resembling that of the expression in (7), total output voltage noise of RFout1 depends on output loads R1 and C1. With the same behavior as the other output, increasing the resistance R1 increases the overall noise. Also, output capacitance C1 has a large effect on the output noise performance. Dynamic range for the RFout1 output side is

determined as

$$DR_1 = 10log\frac{P_{signal}}{P_{noise1}} = 20log\frac{V_{max,rms}}{V_{noise1,rms}} \quad (14)$$

$$DR_1 = 10log\frac{{V_{DD}}^2 \cdot C1}{k_B T[1+\gamma(g_m+g_{mb})R1]} \quad dB \quad (15)$$

With loads for the two output nodes assumed to be equal, that is R1 = R2 and C1 ≈ C2, the two dynamic ranges would be equal. Noise performance in terms of the dynamic range is an important design consideration since it determines the vulnerability of the active balun to unwanted signal like noise. Hence it is critically important that the differential active balun transformer circuit contributes as little noise as possible in the system level design of radio frequency (RF) applications.

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